

PRESS INFORMATION

- FOR IMMEDIATE RELEASE -

Avnet Memec features Lattice ultra-low phase noise, zero-delay buffer clock family

Poing, 10th March, 2009 – Avnet Memec, the highly specialised semiconductor distributor of Avnet Electronics Marketing EMEA, extends its portfolio with Lattice's ispClock™5400D family of differential clock distribution ICs, featuring the CleanClock™ ultra-low phase noise PLL. The ispClock5400D family contains the six-output ispClock5406D and ten-output ispClock5410D. The FlexiClock™ output section of the ispClock5400D devices supports multiple logic standards and dual skew control features. The configuration of each device is held in on-chip non-volatile memory that is reprogrammable through a JTAG interface. Certain aspects of the device can be modified on the fly via an I2C interface. Design for the devices is supported in the Lattice PAC-Designer® software tool.

The ispClock5400D family enables designers to reduce cost and complexity in their differential clock networks while providing the flexibility for late design changes, even after board assembly. Typical applications that benefit from the ispClock5400D devices include supplying high quality reference clocks to high speed serialized communication ICs that use SERDES technology, and the consolidation of components, such as fan-out buffers and zero-delay buffers, typically used for distributing high frequency clocks in a circuit board.

CleanClockPLL

The ispClock5400D devices integrate an ultra-low phase noise CleanClock PLL, including an on-chip programmable analog filter and a programmable VCO with input clock frequencies up to 400MHz. The PAC-Designer software tool automatically determines the parameters of the PLL depending on the input and output clock frequencies. This wide band CleanClock PLL is compatible with the Spreadspectrum clocks required for distributing PCI Express and SATA clocks. The phase noise of the PLL is low enough to be suitable for sourcing clocks to SERDES chips.

FlexiClock Outputs

The ispClock5400 family provides in-system programmable FlexiClock differential outputs. Each output can be configured to interface with a number of logic standards such as LVDS, MLVDS, HCSL, LVPECL, HSTL and SSTL. The output clock can be individually skewed using the phase angle and time skew mechanisms. In addition, the skew can be changed dynamically in-system through an I²C interface.

Timing Adjustments after Board Assembly

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Typical ispClock5400D Applications

SERDES Reference Clock Source

The need for a reference clock source for FPGAs and ASSPs with SERDES (such as the new LatticeECP3™ FPGA family also introduced today) traditionally has been addressed by expensive crystal oscillators with differential outputs. The ispClock5400D device enables the use of a lower cost, lower frequency CMOS oscillator clock source, reducing the overall cost of implementation because the cost of a differential interface oscillator is higher than a CMOS Oscillator and the ispClock5406D device together.

Simple Low-cost Differential Clock Distribution Solution

Clock distribution requirements are determined by the type of logic interface, frequency, jitter and number of outputs. Discrete off-the-shelf clock distribution buffers provide point solutions for each of these. However, a typical system with multiple cards requires many types of clock distribution buffers from different vendors, resulting in a more expensive bill of material and increased inventory management costs. Because the ispClock5400D devices can be programmed as a fan-out buffer or a zero-delay buffer along with a number of outputs, they can satisfy diverse clock distribution requirements. The resulting design is not only lower in cost but also enables designers to compensate for timing errors due to trace lengths or other device related timing variations. Consequently, designers can standardize on ispClock5400D devices across all of their designs.

Software Support

ispClock5400D designs can be implemented using an intuitive and user-friendly GUI provided in the PAC-Designer version 5.0 software tool. The PAC-Designer 5.0 tool can be downloaded for free from the Lattice website, www.latticesemi.com/pac-designer

Availability

Samples of the ispClock5406D device (48-pin QFNS package) and ispClock5410D device (64-pin QFNS package) are available immediately.

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About Avnet Memec

Avnet Memec, an independent business unit of Avnet Electronics Marketing EMEA, is a highly specialised semiconductor distributor, operating on a pan-European basis and employing a significant number of engineers to support customers' design efforts. Avnet Memec specialises in highly innovative suppliers and technologies, which will help a variety of customers to differentiate their designs. Its area of specialisation extends from Analog and Microcontrollers to RF, Datacom and Networking. The company operates from 30 offices in 17 European countries and represents major semiconductor franchises on a pan-European basis. Its many major supplier partners include Cirrus Logic, Lattice, Marvell, NEC, and Silicon Laboratories. The company's Web site is located at www.avnet-memec.eu

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